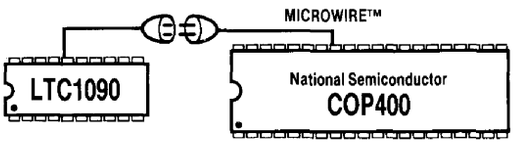
Interfacing the LTC1090 to the COP402N MCU

Guy Hoover
William Rempfer



Introduction

This application note describes the hardware and software required for communication between the LTC1090 10-bit data acquisition system and the National Semiconductor COP400 microcontroller family which uses the MICROWIRE serial interface. The simple four wire interface is capable of completing a 10-bit conversion and shifting the data in 100μs. Configuration of the LTC1090 and the COP402N will be discussed as it applies to this interface. Schematics, code, and timing diagrams will be shown. Finally, a summary of the key points of this interface will be given including data throughput rates.

Interface Details

The LTC1090 has two clock lines: ACLK and SCLK. ACLK controls the A/D conversion rate while SCLK controls the data shift rate. Data is transferred in a full duplex format over D_{IN} and D_{OUT}.

The National Semiconductor MICROWIRE interface is a synchronous, full duplex, serial port built into the COP400 family that allows the user to easily interface to the LTC1090. MICROWIRE provides clock, data in and data out lines that are compatible with the LTC1090. One additional line (G0) is required to control the $\overline{CS}$ pin on the LTC1090. The schematic of Figure 1 shows how the two devices are connected.

Hardware Description

The actual interface will involve using the COP402N, a member of the COP400 family. All code shown here should work with any of the COP400 family.

The code for this interface was developed on a COP400 evaluation board which allows an external EPROM to be used in place of the internal processor ROM.

The timing diagram of Figure 2 was obtained with an HP1631A logic analyzer using a 2MHz ACLK. The COP402N clock was 4MHz.

The analog section of the schematic in Figure 1 is omitted for clarity. For a complete discussion of the analog considerations involved in using the LTC1090 please see the data sheet.

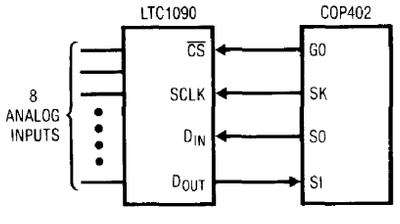


Figure 1. Schematic

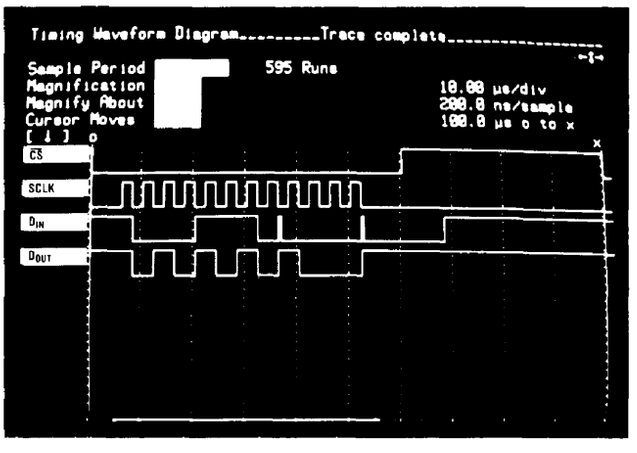


Figure 2. Timing Diagram

Software Description

The software configures and controls the MICROWIRE serial interface of the COP402N. Additionally, the software manipulates G0 ($\overline{CS}$ of the LTC1090) and generates a delay during which time the LTC1090 performs a conversion.

The code first initializes the B register and then loads the LTC1090 D_{IN} word into the RAM of the COP402 one nibble at a time. As shown in Figure 3 the D_{IN} word configures the LTC1090 for CH0 with respect to COM, unipolar, MSB first, and 12 bits. SO is configured as an output. The carry is set so that when an XAS instruction is generated the shift clock (SK) will begin clocking data.

The first nibble of the D_{IN} word is loaded into the ACC and G0 ($\overline{CS}$) is cleared. The D_{IN} nibble is loaded into the shift register and the data begins to shift. The second nibble of the D_{IN} word is loaded into the ACC. One NOP is allowed for timing and then the contents of the ACC are swapped with those of the shift register. The MSBs of the LTC1090 D_{OUT} word are now in the ACC. This data is then stored in memory location $13. The ACC is loaded with null data from RAM and another swap between the ACC and the shift register is executed. The next D_{OUT} nibble is stored in $14. The carry is cleared so that on the next XAS instruction the shift clock will stop. The XAS instruction is executed and the final nibble of the LTC1090 D_{OUT} word containing the two LSBs and two zeroes is loaded into the

$10				$11			
1	0	0	0	1	1	1	0
S/D	O/S	S1	S2	UNI	MSBF	WL1	WL0

Figure 3. D_{IN} Word for LTC1090

MSB

B9	B8	B7	B6	$13
B5	B4	B3	B2	$14

LSB

B1	B0	0	0	$15

D_{OUT} from LTC1090 stored in COP402 RAM

Figure 4. Memory Map

LABEL	MNEMONIC		COMMENTS
	CLRA		MUST BE FIRST INSTRUCTION
	LBI	1,0	BR = 1 BD = 0 INITIALIZE B REG.
	STII	8	FIRST D_{IN} NIBBLE IN $10
	STII	E	SECOND D_{IN} NIBBLE IN $11
	STII	0	NULL DATA IN $12, B = $13
	LEI	C	SET EN TO (1100) BIN
LOOP	SC		CARRY SET
	LDD	1,0	LOAD FIRST D_{IN} NIBBLE IN ACC
	OGI	50	G0 ($\overline{CS}$) CLEARED
	XAS		ACC TO SHIFT REG. BEGIN SHIFT
	LDD	1,1	LOAD NEXT D_{IN} NIBBLE IN ACC
	NOP		TIMING
	XAS		NEXT NIBBLE, SHIFT CONTINUES
	XIS	0	FIRST NIBBLE D_{OUT} TO $13
	LDD	1,2	PUT NULL DATA IN ACC
	XAS		SHIFT CONTINUES, D_{OUT} TO ACC
	XIS	0	NEXT NIBBLE D_{OUT} TO $14
	RC		CLEAR CARRY
	CLRA		CLEAR ACC
	XAS		THIRD NIBBLE D_{OUT} TO ACC
	OGI	51	G0 ($\overline{CS}$) SET
	XIS	0	THIRD NIBBLE D_{OUT} TO $15
	LBI	1,3	SET B REG. FOR NEXT LOOP

Figure 5. COP402 Code

ACC. G0 ($\overline{CS}$) is taken high and the A/D begins its next conversion cycle. The third D_{OUT} nibble is stored in location $15. The B register is then reinitialized so that when the loop is run again the data will always be stored in the same memory locations. The D_{OUT} data from the LTC1090 is now in a left justified format as shown in Figure 4.

44 ACLK cycles must be allowed between transfers for the A/D to perform its next conversion. The instructions, after G0 is set, take enough time so that no additional delay is required by this program.

Summary

A four wire interface between the LTC1090 and the COP402N with a combined data conversion and transfer time of 100μs was demonstrated. The interface used the MICROWIRE serial port of the COP402N. The 10 data bits of the LTC1090 are shifted MSB first in three four bit transfers with the last two bits filled with zeroes. The data is stored left justified in the COP402N's internal RAM. The code demonstrated will work on any member of the COP400 family.

MICROWIRE is a trademark of National Semiconductor Corp.